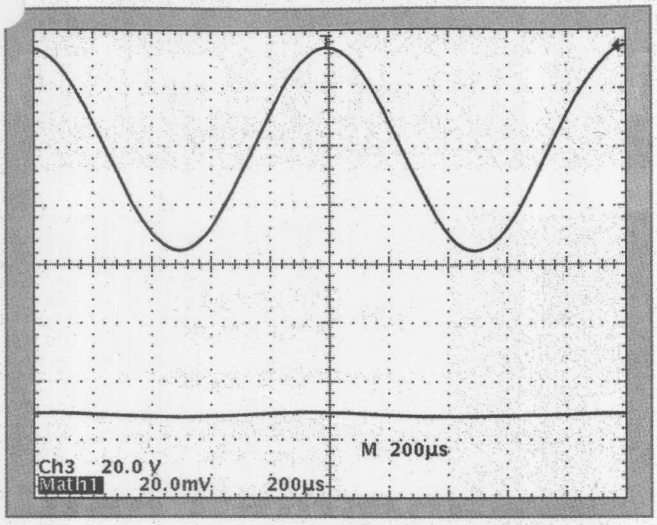
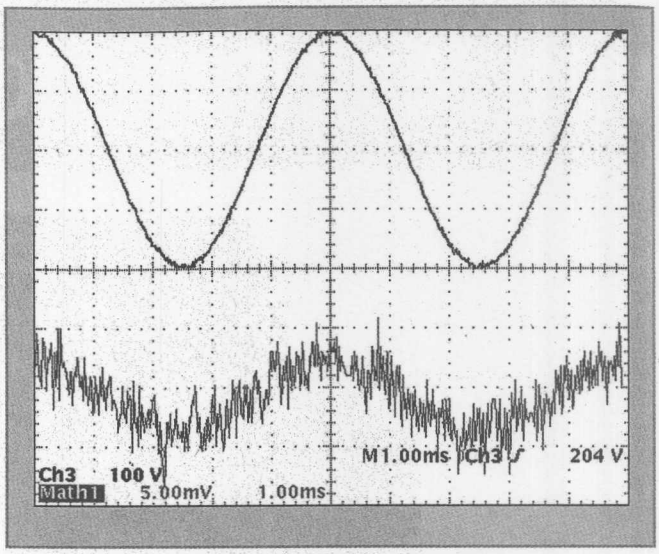
can be used for larger common-mode signals. Figure 4 shows that the system can reject a 400-V p-p common-mode signal (upper waveform), with the residual error of less than 10 mV p-p shown in the lower waveform.



3. With a 5-V power supply and a 1-kHz, 60-V p-p common-mode signal (upper trace), the circuit's output (lower trace) illustrates the high common-mode rejection.



4. Using a ±15-V supply, the circuit reduces a 400-V p-p common-mode signal (upper trace) to under 10 mV p-p (lower trace).

Simple Technique Generates Precise HART Waveforms

Anthony H. Smith

Scitech, 129 Deep Spinney, Biddenham, Bedfordshire, MK40 4QJ England

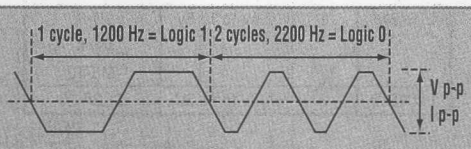
CIRCLE 522

Designed to complement conventional 4- to 20-mA analog signaling, the Highway Addressable Remote Transducer (HART) protocol supports two-way digital communications for process measurement and control devices. The protocol uses frequency-shift keying (FSK), with the digital signal made up of two frequencies—1200 Hz representing ones and 2200 Hz representing zeros. Because the average FSK-signal value is always zero, the 4- to 20-mA analog signal isn't affected.

Ideally, sinewaves of these two frequencies would be superimposed on the dc analog signal to provide simultaneous analog and digital communication. However, generating phase-continuous FSK sinewaves is not a simple matter. So the HART physical-layer specification allows for a more generalized waveform whose shape, amplitude, and rate-of-change must fall within defined limits. A trapezoidal waveform well suits the application *(Fig. 1)*. The limiting values of the parameters are detailed in the table.

The circuit shown in Figure 2 provides a low-cost solution for generating the HART waveform and superimposing it onto a variable dc level. The HART FSK signal fed to the first NAND is gated by the active-high ENABLE signal.

Resistors R4 and R5 split the 5-V rail to form a 2.5-V reference potential, V_{REF}. When ENABLE is low, IC1b's output is low, IC1c's output is high, and because R1 = R2, and assuming the NAND outputs swing rail-to-rail, the voltage V_{IN} at IC2a's noninverting input also sits at 2.5 V.



Parameter	Minimum value	Maximum value
V p-p (V)	0.4	0.6
I p-p (mA)	0.8	1.2
Rate of change at 1200 Hz	1 V/ms (2 mA/ms)	4 V/ms (8 mA/ms)
Rate of change at 2200 Hz	2 V/ms (4 mA/ms)	4 V/ms (8 mA/ms)

1. A typical HART trapezoidal waveform is defined by the parameters shown in the table.

When ENABLE is taken high, the outputs of IC1b and IC1c oscillate in phase with each other and invert the FSK squarewave, such that V_{IN} is now a small squarewave swinging symmetrically about V_{REF} with a peak-to-peak amplitude (in volts) given by:

$$V_{IN(P-P)} = V_P \times \frac{R3}{R3 + R1 \,||\, R2}$$

where V_P is the positive supply-rail voltage, nominally 5 V, and R1||R2 is the parallel combination of R1 and R2. With the resistance values shown in the figure, $V_{IN(P-P)}$ is 200 mV—i.e., the signal swings from 2.4 V to 2.6 V.

At the instant that V_{IN} rises to 2.6 V, IC2a's output goes into positive saturation and C3 starts to charge via R6 and R7. Therefore, the voltage V_{HART} on C3 rises linearly until it reaches 2.6 V. At this point, IC2a rapidly comes out of saturation and behaves as a simple follower, holding V_{HART} at 2.6 V.

When V_{IN} falls to 2.4 V, IC2a's

output goes into negative saturation and C3 starts to discharge via R6 and R7. Consequently, V_{HART} now ramps down linearly until it achieves 2.4 V, at which point IC2a comes out of saturation and again acts like a follower, holding V_{HART} at 2.4 V.

The resulting trapezoidal waveform is equal in amplitude to V_{IN} and swings symmetrically about V_{REF}. The trapezoid's rate-of-change (in V/ms) is given by:

$$\frac{dV}{dt} = \frac{(V_{SAT} - V_{HART})/(R6 + R7)}{C3}$$

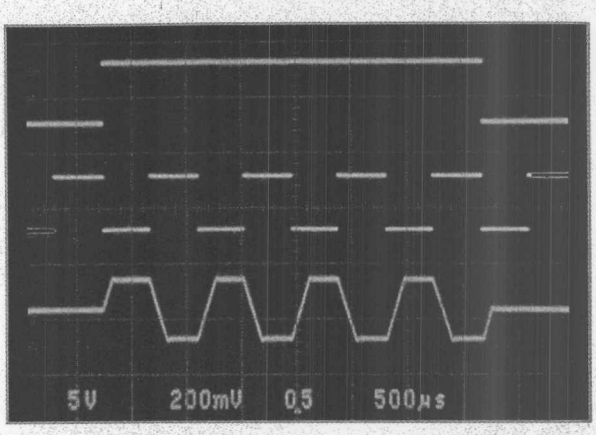
where V_{SAT} is the positive or negative output saturation voltage of IC2a.

Because the ac content of V_{HART} is very small compared to V_{SAT}, it may be approximated by its quiescent level, namely $V_P/2$, or V_{REF}. Also, if IC2a has rail-to-rail output swing, then it is reasonable to assume that its output saturation levels are 5 and 0 V. Therefore, provided that R7 is much smaller than R6, the expression for the rate-of-change (in V/ms) may be simplified to:

$$\frac{dV}{dt} = \frac{\pm V_{REF}}{R6 \times C3}$$

Thus, with values for R6 and C3 as shown in Figure 2, we find that the trapezoid slews at ±1.25 V/ms. If we take the peak-to-peak amplitude of V_{HART} (200 mV) as being equivalent to a HART current signal of 1 mA p-p, the 1.25-V/ms slew rate is equivalent to 6.25 mA/ms in the HART current signal. This sits nicely within the limits quoted in the table.

Note that R7 is necessary to isolate IC2a from the pole introduced by C3, thereby maintaining closed-loop stability. The required value depends on IC2's bandwidth and the value of C3, and it should be chosen to provide optimum waveshape without incurring any ringing or overshoot on V_{HART}. IC2 must be a reasonably wideband device able to slew much faster than the HART trapezoid. The dual LM6132 provides fast, rail-to-rail output while drawing moderate supply current. Other devices like the MAX4126 are equally suitable.



3. A scope display shows the relevant waveforms of the HART signal generator. Top trace: ENABLE signal (5 V/div.). Middle trace: 1200-Hz FSK squarewave (5 V/div.). Bottom trace: output signal, V_O (200 mV/div.). The timebase is 500 µs/div.

The second half of IC2 is used to superimpose the HART signal onto a variable dc level, V_{DC}.

The voltage at IC2b's output, V_O, (in volts) is given by:

$$V_O = \left(1 + \frac{R11}{R8}\right) \times \left(V_{REF} \times \frac{R10}{R9 + R10} + V_{DC} \times \frac{R9}{R9 + R10}\right) - V_{HART} \times \frac{R11}{R8}$$

By making R8 to R11 equal in value, the expression simplifies to:

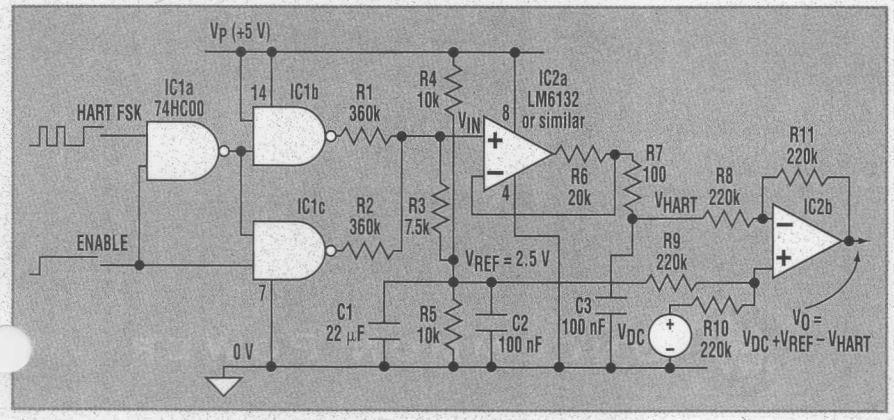
$$V_O = V_{REF} + V_{DC} - V_{HART} \text{ (in volts)}$$

Because V_{HART} consists of a 200-mV trapezoid swinging symmetrically about V_{REF}, the output (V_O) contains only the small HART waveform riding on the variable DC level. By feeding V_O to a suitable voltage-to-current converter, each 200 mV of V_{DC} is equivalent to 1 mA of current. Thus, varying V_{DC} from 0.8 V to 4.0 V is equivalent to a 4- to 20-mA current range.

Resistors R8 to R11 should be much larger than R6 to ensure that they negligibly affect C3's charging current. However, they must not be too large. Otherwise, IC2b's input offset current may introduce errors. If the resistor values are well matched, V_{REF} disappears completely from V_O, such that any inequality in R4 and R5, and/or variations in V_P have minimal effect on the dc content of V_O.

The scope photo in Figure 3 shows how the output at V_O responds to the ENABLE signal. Initially, V_O sits at the level set by V_{DC}. Then when ENABLE goes high, the output ramps between the HART levels in response to the 1200-Hz squarewave. When ENABLE goes low, the output ramps cleanly back to the quiescent dc level.

Although developed for HART-compatible instrumentation, the circuit could be adapted for other applications where it's necessary to limit the slew rate of a signal while maintaining precise control of its amplitude.



2. This circuit converts an FSK squarewave into a trapezoidal waveform and superimposes it onto a variable dc level.

ifd winners

Tied:

Jerry Steele, Maxim Integrated Products, "Read Temperature With One Digital Output And One Digital Input," March 4, 2002.

Saurav Gupta and Monika Sardana, Linear Integrated Circuits Lab, Department of Electronics and Communications, NSIT, New Delhi, India, "High-Q Bandpass Filter Is Well-Suited To Current-Mode Signal Processing," March 4, 2002.